REMARKS

The Applicants have received and reviewed the final Office Action mailed June 19, 2007 and the Advisory Action mailed August 28, 2007. An RCE was filed on September 11, 2007. Claims 1 - 3 and 7 - 9 remain pending in the application. Claims 1, 2, 7 and 9 have been amended by the amendment being submitted herewith. Claim 4 - 6 and 10 - 11 were cancelled in a previously filed Response and Amendment. Claims 1 - 3 and 7 - 9 stand rejected. The Applicants respectfully request reconsideration.

Rejection Under 35 U.S.C. §102(b)

The Examiner rejected claims 1 - 2 and 7 - 9 under 35 U.S.C. §102(b) as being anticipated by Doh et al. The Applicants respectfully traverse the rejection for at least the following reasons.

The arguments made by the Applicants in the previously filed Responses are incorporated herein. As previously argued by the Applicants, Doh et al. does not teach a photodetector coupled to a gain stage, which is directly coupled to a clock and data recovery circuit (CDR) circuit, as recited in independent claim 1 of the present application. To the contrary, in the two figures that show the make up of receivers in Doh et al., both of them show the photodetector (11 in Fig. 1 and 110 in Fig. 3) being coupled to a low noise amplifier (12 in Fig. 1 and 120 in Fig. 3), which is coupled to a limiting amplifier (13 in Fig. 1 and 130 in Fig. 3), which is coupled to a CDR circuit (15 in Fig. 1 and 180 in Fig. 3). Thus, Doh et al. clearly teach using multiple gain stages (12 and 13 in Fig. 1; 120 and 130 in Fig. 3). Nowhere in Doh et al. is there any suggestion or teaching of eliminating either of the gain stages.

In contrast, in accordance with the invention, it has been determined that the limiting amplifier can be eliminated and the transimpedance amplifier (TIA) can be coupled to a CDR circuit. This feature of the invention allows a lower bandwidth, and therefore less expensive, TIA to be used in the receiver module. Because the TIA has a lower bandwidth, it can also be made to have a higher gain, which obviates the need for the limiting amplifier following the TIA. Removing the limiting amplifier reduces the overall power consumption of the receiver. In addition, because the CDR circuit can be operated at a lower power supply than the limiting amplifier, this also reduces power consumption requirements.

These features are not taught or suggested by the prior art of record because the prior art of record does not recognize that these advantages are made possible by coupling the TIA directly to the CDR circuit. Due to the regenerative qualities of a CDR circuit, it can tolerate more jitter at its input than a limiting amplifier, which enables the bandwidth of the TIA to be reduced. This clearly is not taught or suggested by Doh et al. because, as stated above, Doh et al. discloses using two gain stages 12, 13 and 120, 130.

In rejecting claim 1, the Examiner states that the gain stage recited in claim 1 corresponds to components 12 and 13 in Doh et al. In paragraph 0003 of Doh et al., component 12 is described as a TIA. In paragraph 0004 of Doh et al., component 13 is described as a limiting amplifier. Nevertheless, the Examiner has interpreted the combination of components 12 and 13 as the "gain stage" recited in independent claim 1. Despite Applicants' previous arguments that components 12 and 13 do not constitute a "gain stage", as recited in claim 1, the Examiner has maintained the rejection. However, the rejection is flawed for at least the following reasons.

Claim 2 of the present application further limits claim 1 by reciting that the "gain stage is a transimpedance amplifier circuit". In rejecting claim 2, the Examiner cites the language from paragraph 0003 of Doh et al. finding that component 12 shown in Fig. 1 of Doh is a transimpedance amplifier circuit. The Applicant respectfully submits that this is improper claim construction on the part of the Examiner. The Examiner has made two completely inconsistent findings, namely, that (1) the "gain stage" recited in claim 1 corresponds to components 12 and 13 in Doh et al., and (2) that the same "gain stage" recited in claim 2 with reference to claim 1 corresponds only to component 12 in Doh et al. The Applicants respectfully submit that the Examiner's claim construction is improper.

The Examiner has made this improper claim construction because claim 1 states that the gain stage is coupled to the photodetector and to the CDR circuit. Therefore, the only way that the Examiner's rejection of claim 1 under 35 U.S.C. §102(b) can be made based on Doh et al. is if the Examiner construes the gain stage in claim 1 as corresponding to the multiple gain stages 12 and 13 disclosed in Doh et al., since gain stage 12 is coupled to a photodetector and gain stage 13 is coupled to a CDR circuit. Likewise, the only way that the Examiner's rejection of claim 2 under 35 U.S.C. §102(b) can be made based on Doh et al. is if the Examiner construes the gain stage in claim 2 as corresponding to the single gain stage 12 disclosed in Doh et al. This is improper claim construction because claim 2 requires the gain stage being directly coupled to the

CDR circuit, and gain stage 13 in Doh et al., not gain stage 12, is coupled to the CDR circuit of Doh et al. Accordingly, the Applicants respectfully submit that the rejection is improper and request that it be withdrawn.

Furthermore, in order to clarify the invention, claim 1 has been amended to substitute "a transimpedance amplifier circuit" in the place of the "gain stage". Because claim 1 as amended recites that the transimpedance amplifier is coupled to the photodetector and to the CDR circuit, it is clear that claim 1 is not anticipated by Doh et al. For this additional reason, the Applicants respectfully submit that claim 1 is patentable over Doh et al. and respectfully request that the rejection be withdrawn. For at least the reason that claims 2 and 3 depend directly or indirectly from claim 1, and therefore incorporate the elements thereof, these claims are also patentable over Doh et al. Accordingly, the Applicants respectfully request that the rejection of these claims also be withdrawn.

The Examiner has rejected independent claim 7 using the same improper claim construction described above with reference to the rejection of claim 1. Claim 7 recites extracting clock information from the voltage signal converted by the gain stage from the current signal, which is not taught or suggested by Doh et al. Doh et al. teaches extracting clock information from a voltage signal output by gain stage 13 (i.e., from the limiting amplifier), not from gain stage 12 (i.e., the transimpedance amplifier). For the reasons described above with reference to the rejection of claim 1, the Applicants respectfully submit that independent claim 7 is patentable over Doh et al., and respectfully requests that this rejection be withdrawn.

In addition, to further clarify the invention, claim 7 has been amended to substitute "a transmimpedance amplifier circuit" in the place of the "gain stage". Clearly, Doh et al. does not teach or suggest extracting clock information from the transimpedance amplifier 12, but rather, teaches extracting clock information from the limiting amplifier 13. For this additional reason, the Applicants respectfully submit that claim 7 is patentable over Doh et al. and respectfully request that the rejection of claim 7 as unpatentable over Doh et al. be withdrawn.

For at least the reason that claims 8 and 9 depend directly or indirectly from claim 7, and therefore incorporate the elements thereof, the Applicants respectfully submit that claims 8 and 9 are also patentable over Doh et al., and respectfully request that the rejection of these claims also be withdrawn.

Rejection Under 35 U.S.C. §103(a)

The Examiner rejected claims 3 – 6, 10 and 11 under 35 U.S.C. §103(a). The Applicants respectfully traverse the rejection for at least the following reasons.

For at least the reason that these claims depend directly or indirectly from either of independent claims 1 or 7, and therefore incorporate the elements thereof, the Applicants respectfully submit that these claims are also patentable over Doh et al., or over Doh et al. in view of Swenson et al., and respectfully request that the rejection of these claims also be withdrawn.

Furthermore, with respect to the Examiner's rejection of claim 3, the Applicants disagree that it would be obvious to implement a transimpedance amplifier and a CDR circuit in the same integrated circuit package, or chip, at least because a limiting amplifier is normally interposed between the CDR circuit and the transimpedance amplifier, as taught by both Doh et al. and Swenson et al. Therefore, it would not be obvious to implement these circuits on a single chip merely because there are well known "benefits of integration of circuits on a single chip", as contended by the Examiner. For this additional reason, the Applicants respectfully submit that claim 3 is patentable over Doh et al. and respectfully request that the rejection be withdrawn.

CONCLUSION

For the reasons set forth above, the Applicants respectfully submit that all pending claims are in condition for allowance. The Applicants respectfully request reconsideration of the rejections and allowance of the application. Should there be any further questions or concerns, the Examiner is urged to telephone the undersigned to expedite prosecution.

Respectfully submitted,
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